WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate of semiconductor material, said substrate having a well formed therein;

at least three substantially spiral inductors formed within said well, said inductors being arranged in said well such that each of said inductors is inductively coupled to at least one other of said inductors; and

a respective pair of input/output terminals for each of said inductors.

2. The semiconductor device of claim 1 wherein:

each of said inductors has a center; and

said centers are substantially aligned along an axis.

3. The semiconductor device of claim 2 wherein:

said first inductor has a first number of turns;

said second inductor has a second number of turns; and

said third inductor has a third number of turns.

4. The semiconductor device of claim 3 wherein said first, second and third numbers are equal.

5. The semiconductor device of claim 4 wherein:

said semiconductor device has a major surface defining a plane; and

said well is formed in said major surface.

6. The semiconductor device of claim 5 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

7. The semiconductor device of claim 5 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

8. The semiconductor device of claim 7 wherein said side wall is at an angle of about 54.74° relative to said plane.

9. The semiconductor device of claim 3 wherein:

said semiconductor device has a major surface defining a plane; and

said well is formed in said major surface.

10. The semiconductor device of claim 9 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

11. The semiconductor device of claim 9 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

12. The semiconductor device of claim 11 wherein said side wall is at an angle of about 54.74° relative to said plane.

13. The semiconductor device of claim 2 wherein:

said semiconductor device has a major surface defining a plane; and

said well is formed in said major surface.

14. The semiconductor device of claim 13 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

15. The semiconductor device of claim 13 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

16. The semiconductor device of claim 15 wherein said side wall is at an angle of about 54.74° relative to said plane.

17. A coupled inductor structure having a high quality factor, said structure comprising:

a substrate of semiconductor material, said substrate having a well formed therein;

at least three substantially spiral inductors formed within said well, said inductors being arranged in said well such that each of said inductors is inductively coupled to at least one other of said inductors; and

a respective pair of input/output terminals for each of said inductors.

18. The coupled inductor structure of claim 17 wherein:

each of said inductors has a center; and

said centers are substantially aligned along an axis.

19. The coupled inductor structure of claim 18 wherein:

said first inductor has a first number of turns;

said second inductor has a second number of turns; and

said third inductor has a third number of turns.

20. The coupled inductor structure of claim 19 wherein said first, second and third numbers are equal.

21. The coupled inductor structure of claim 20 wherein:

said semiconductor device has a major surface defining a plane; and

said well is formed in said major surface.

22. The coupled inductor structure of claim 21 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

23. The coupled inductor structure of claim 21 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

24. The coupled inductor structure of claim 23 wherein said side wall is at an angle of about 54.74° relative to said plane.

25. The coupled inductor structure of claim 18 wherein:

said semiconductor device has a major surface defining a plane; and

said well is formed in said major surface.

26. The coupled inductor structure of claim 25 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

27. The coupled inductor structure of claim 25 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

28. The coupled inductor structure of claim 27 wherein said side wall is at an angle of about 54.74° relative to said plane.

29. The coupled inductor structure of claim 17 wherein:

said semiconductor device has a major surface defining a plane; and

said well is formed in said major surface.

30. The coupled inductor structure of claim 29 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

31. The coupled inductor structure of claim 29 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

32. The coupled inductor structure of claim 31 wherein said side wall is at an angle of about 54.74° relative to said plane.

33. A signal splitting and combining circuit comprising:

a substrate of semiconductor material, said substrate having a well formed therein;

at least three substantially spiral inductors formed within said well, said inductors being arranged in said well such that each of said inductors is inductively coupled to at least one other of said

inductors, a third one of said inductors being coupled between first and second ones of said inductors; and

a respective pair of input/output terminals for each of said inductors; wherein:

when respective first and second signals are input to each of first and second ones of said pairs of input/output terminals, a sum of multiples of said first and second signals is output on a third one of said pairs of input/output terminals; and

when an input signal is input on said third one of said pairs of input/output terminals, respective first and second output signals are output on respective ones of said first and second pairs of input/output terminals, said input signal being a sum of multiples of said first and second output signals.

34. The signal splitting and combining circuit of claim 33 wherein:

each of said inductors has a center; and

said centers are substantially aligned along an axis.

35. The signal splitting and combining circuit of claim 34 wherein:

said first inductor has a first number of turns;

said second inductor has a second number of turns; and

said third inductor has a third number of turns; wherein:

when said respective first and second signals are input to each of said first and second ones

of said pairs of input/output terminals, said sum of multiples of said first and second signals is a sum of (a) a product of said first signal and a ratio of said third number of turns to said first number of turns, and (b) a product of said second signal and a ratio of said third number of turns to said second number of turns; and

when said input signal is input on said third one of said pairs of input/output terminals, said input signal is a sum of (a) a product of said respective first output signal and a ratio of said first number of turns to said third number of turns, and (b) a product of said respective second output signal and a ratio of said second number of turns to said third number of turns.

36. The signal splitting and combining circuit of claim 35 wherein said first, second and third numbers are equal; wherein each of said multiples is one.

37. The signal splitting and combining circuit of claim 36 wherein:

said semiconductor substrate has a major surface defining a plane; and

said well is formed in said major surface.

38. The signal splitting and combining circuit of claim 37 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

39. The signal splitting and combining circuit of claim 37 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

40. The signal splitting and combining circuit of claim 39 wherein said side wall is at an angle of about 54.74° relative to said plane.

41. The signal splitting and combining circuit of claim 35 wherein:

said semiconductor substrate has a major surface defining a plane; and

said well is formed in said major surface.

42. The signal splitting and combining circuit of claim 41 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

43. The signal splitting and combining circuit of claim 41 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

44. The signal splitting and combining circuit of claim 43 wherein said side wall is at an angle of about 54.74° relative to said plane.

45. The signal splitting and combining circuit of claim 34 wherein:

said semiconductor substrate has a major surface defining a plane; and

said well is formed in said major surface.

46. The signal splitting and combining circuit of claim 45 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

47. The signal splitting and combining circuit of claim 45 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

48. The signal splitting and combining circuit of claim 47 wherein said side wall is at an angle of about 54.74° relative to said plane.

49. A method of forming a coupled inductor structure in a semiconductor substrate having a surface, said method comprising:

forming a well in said surface of said substrate, said well having a bottom and a side wall;

depositing a first insulating layer on said bottom of said well;

depositing a first lead-in conductor over said first insulating layer;

depositing a second insulating layer over said first lead-in conductor;

depositing a first spiral inductor over said second insulating layer in contact with said first lead-in conductor;

forming a first termination wire conducting between said first spiral inductor and said surface;

depositing a third insulating layer over said first spiral inductor;

depositing a second lead-in conductor over said third insulating layer;

depositing a fourth insulating layer over said second lead-in conductor;

depositing a second spiral inductor over said fourth insulating layer in contact with said second lead-in conductor;

forming a second termination wire conducting between said second spiral inductor and said surface;

depositing a fifth insulating layer over said second spiral inductor;

depositing a third lead-in conductor over said fifth insulating layer;

depositing a sixth insulating layer over said third lead-in conductor;

depositing a third spiral inductor over said sixth insulating layer in contact with said third lead-in conductor;

forming a third termination wire conducting between said third spiral inductor and said surface;

depositing a seventh insulating layer over said third spiral inductor.

50. The method of claim 49 wherein said forming said well comprises forming said well with said side wall substantially perpendicular to said surface.

51. The method of claim 49 wherein said forming said well comprises forming said well with said side wall at an oblique angle relative to said surface.

52. The method of claim 51 wherein said oblique angle is about 54.74°.

53. The method of claim 49 wherein said depositing of any of said lead-in conductors comprises electroplating.

54. The method of claim 53 wherein said depositing of any of said spiral inductors comprises electroplating.

55. The method of claim 54 wherein said forming of any one said termination wires comprises electroplating.

56. The method of claim 49 wherein said depositing of any of said spiral inductors comprises electroplating.

57. The method of claim 56 wherein said forming of any one said termination wires comprises electroplating.

58. The method of claim 49 wherein said forming of any one said termination wires comprises electroplating.